

CLAIMS

What is claimed is:

- 1 1. A re-targetable communication processor, comprising:
 - 2 a. a connectivity unit;
 - 3 b. a digital signal processing core coupled to the connectivity unit;
 - 4 c. a plurality of scaleable functional units, coupled to the connectivity unit, to
 - 5 execute mathematically intensive operations, further including:
 - 6 a local memory;
 - 7 a plurality of removable complex arithmetic elements (hereinafter
 - 8 CAE) coupled to one another, to the local memory and to an inter-
 - 9 CAE bus; and
 - 10 a bus controller coupled to the inter-CAE bus and the connectivity
 - 11 unit.

- 1 2. The re-targetable communication processor according to claim 1, the CAE
 - 2 further comprising:
 - 3 a. a CAE memory to store data for the mathematically intensive operations;
 - 4 b. a sequencer, coupled to an arithmetic unit, a data router and the CAE
 - 5 memory, to generate addresses and control information;

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- 6 c. the arithmetic unit, coupled to the CAE memory and the data router,
 7 optimized to execute operations in accordance with the control information;
 8 and
 9 d. the data router to route data to the sequencer and the CAE memory and to
 10 facilitate communications among the CAEs in the scaleable functional unit.

- 1 3. The re-targetable communication processor according to claim 2, the CAE
 2 memory further comprising:
 3 two banks of separately addressable data memories.

- 1 4. The re-targetable communication processor according to claim 3, the arithmetic
 2 unit further comprising:
 3 a. a register file to accept data from the data memories; and
 4 b. a plurality of multiplier-accumulator engines, coupled to one another, to the
 5 register file and to the data memories, to operate on the mathematically
 6 intensive operations.

- 1 5. The re-targetable communication processor according to claim 4, the multiplier-
 2 accumulator engine further comprising:

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- 3 a. a pre-adder to generate a first sum by adding data from the register file and
4 the data memory;
- 5 b. a multiplier to generate a multiplier output by multiplying data from the data
6 memories or the first sum;
- 7 c. an accumulator to generate a second sum by adding the multiplier output or
8 data from the data memories; and
- 9 d. a data packing block to configure the second sum into a pre-defined format.
- 1 6. The re-targetable communication processor according to claim 5, the multiplier
2 further including a programmable shifter.
- 1 7. The re-targetable communication processor according to claim 1, the CAEs are
2 coupled to one another via an east port, a west port and the inter-CAE port.
- 1 8. The re-targetable communication processor according to claim 1, further
2 including a micro-controller core coupled to the connectivity unit.
- 1 9. The re-targetable communication processor according to claim 2, wherein a first
2 delay introduced by the sequencer matches a second delay introduced by the
3 arithmetic unit.

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- 1 10. A scalable functional unit in a re-targetable communication processor,
2 comprising:
3 a. a local memory;
4 b. a plurality of removable complex arithmetic elements (hereinafter CAE)
5 coupled to one another, to the local memory and to an inter-CAE bus; and
6 c. a bus controller coupled to the inter-CAE bus and the connectivity unit.
- 1 11. The scalable functional unit according to claim 10, the CAE further comprising:
2 a. a CAE memory to store data for the mathematically intensive operations;
3 b. a sequencer, coupled to an arithmetic unit, a data router and the CAE
4 memory, to generate addresses and control information;
5 c. the arithmetic unit, coupled to the CAE memory and the data router,
6 optimized to execute operations in accordance with the control information;
7 and
8 d. the data router to route data to the sequencer and the CAE memory and to
9 facilitate communications among the CAEs in the scalable functional unit.
- 1 12. The scalable functional unit according to claim 11, the CAE memory further
2 comprising:

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3 two banks of separately addressable data memories.

1 13. The scaleable functional unit according to claim 12, the arithmetic unit further
2 comprising:

- 3 a. a register file to accept data from the data memories; and
4 b. a plurality of multiplier-accumulator engines, coupled to one another, to the
5 register file and to the data memories, to operate on the mathematically
6 intensive operations.

1 14. The scaleable functional unit according to claim 13, the multiplier-accumulator
2 engine further comprising:

- 3 a. a pre-adder to generate a first sum by adding data from the register file and
4 the data memory;
5 b. a multiplier to generate a multiplier output by multiplying data from the data
6 memories or the first sum;
7 c. an accumulator to generate a second sum by adding the multiplier output or
8 data from the data memories; and
9 d. a data packing block to configure the second sum into a pre-defined format.

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1 15. The scaleable functional unit according to claim 14, the multiplier further
2 including a programmable shifter.

1 16. The scaleable functional unit according to claim 10, the CAEs are coupled to one
2 another via an east port, a west port and the inter-CAE port.

1 17. The scaleable functional unit according to claim 11, wherein a first delay
2 introduced by the sequencer matches a second delay introduced by the arithmetic
3 unit.

1 18. A computer system, comprising:
2 a microprocessor coupled to a system bus;
3 a system controller coupled to the system bus; and
4 an input/output controller hub, coupled to the system controller and coupled to an
5 input/output bus;
6 an add-in card, coupled to the input/output bus, further including:
7 a re-targetable communication system, comprising:
8 a. a connectivity unit;
9 b. a digital signal processing core coupled to the connectivity unit;

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c. a plurality of scaleable functional units, coupled to the connectivity unit, to execute mathematically intensive operations, further including:

- i. a local memory;
- ii. a plurality of removable complex arithmetic elements (hereinafter CAE) coupled to one another, to the local memory and to an inter-CAE bus; and
- iii. a bus controller coupled to the inter-CAE bus and the connectivity unit.

19. The computer system according to claim 18, the CAE further comprising:
- a. a CAE memory to store data for the mathematically intensive operations;
 - b. a sequencer, coupled to an arithmetic unit, a data router and the CAE memory, to generate addresses and control information;
 - c. the arithmetic unit, coupled to the CAE memory and the data router, optimized to execute operations in accordance to the control information; and
 - d. the data router to route data to the sequencer and the CAE memory and to facilitate communications among the CAEs in the scaleable functional unit.

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- 1 20. The computer system according to claim 19, the CAE memory further
2 comprising:
3 two banks of separately addressable data memories.

- 1 21. The computer system according to claim 20, the arithmetic unit further
2 comprising:
3 a. a register file to accept data from the data memories; and
4 b. a plurality of multiplier-accumulator engines, coupled to one another, to the
5 register file and to the data memories, to operate on the mathematically
6 intensive operations.

- 1 22. The computer system according to claim 21, the multiplier-accumulator engine
2 further comprising:
3 a. a pre-adder to generate a first sum by adding data from the register file and
4 the data memory;
5 b. a multiplier to generate a multiplier output by multiplying data from the data
6 memories or the first sum;
7 c. an accumulator to generate a second sum by adding the multiplier output and
8 data from the data memories; and
9 d. a data packing block to configure the second sum into a pre-defined format.

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1 23. The computer system according to claim 22, the multiplier further including a
2 programmable shifter.

1 24. The computer system according to claim 18, the CAEs are coupled to one another
2 via an east port, a west port and the inter-CAE port.

1 25. The computer system according to claim 18, wherein the re-targetable
2 communication system further including a micro-controller core that is coupled
3 to the connectivity unit.

1 26. The computer system according to claim 19, wherein a first delay introduced by
2 the sequencer matches a second delay introduced by the arithmetic unit.

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